IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Shibly S. Ahmed et al.	)	Group Art Unit: 2812
	)	
Application No.: 10/602,061	)	Examiner: R. Pompey
	)	
Filed: June 24, 2003	)	
	)	
For: DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	)	

TRANSMITTAL FOR APPEAL BRIEF

U.S. Patent and Trademark Office
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Sir:

Transmitted herewith is an Appeal Brief in support of the Notice of Appeal filed June 3, 2005.

Enclosed is a check for ☐ $250.00 ☒ $500.00 to cover the Government fee.

The Commissioner is hereby authorized to charge any other appropriate fees that may be required by this paper that are not accounted for above, and to credit any overpayment, to Deposit Account No. 50-1070.

Respectfully submitted,

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Date: August 3, 2005

PATENT
Attorney Docket No. H1105D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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APPEAL BRIEF

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401 Dulany Street
Alexandria, Virginia 22314

Sir:

This Appeal Brief is submitted in response to the rejection mailed January 12, 2005 and in support of the Notice of Appeal filed June 3, 2005.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 11-15 and 21-29 are pending in this application. Claims 1-10, 16-20, 30 and 31 have been previously canceled without prejudice or disclaimer. Claims 11-15 and 21-29 are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the Final Office Action mailed January 12, 2005. Appellants note that a Request for Reconsideration was filed March 8, 2005 along with a Declaration under 37 C.F.R. § 1.131. In response to the Request for Reconsideration, an Advisory Action mailed May 4, 2005 was issued. The Advisory Action states that the arguments presented in the Request for Reconsideration were persuasive and overcame the rejection of the pending claims under 35 U.S.C. § 103 based on Yu (U.S. Patent No. 6,458,662) in view of Gambino et al. (U.S. Patent No. 6,689,650).

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Each of the independent claims involved in this appeal is recited below, followed in parenthesis by examples of where support can be found in the specification and drawings for the claimed subject matter. In addition, each dependent claim argued separately below is also summarized.

Claim 11 recites: A method of manufacturing a semiconductor device, comprising: forming a fin structure on an insulating layer, the fin structure including a first side surface, a second side surface, and a top surface and having a thickness ranging from about 300 Å to about 1500 Å (page 5, paragraph 24; page 6, paragraph 27; Figs. 2A and 2B, 210); forming source and drain regions at ends of the fin structure (page 6, paragraph 28; Fig. 2A, 220, 230); depositing a gate material over the fin structure to a thickness ranging from about 300 Å to about 1500 Å, the gate material surrounding the top surface and the first and second side surfaces (page 7, paragraph 31; Fig. 3, 320); etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin (page 7, paragraphs 32-34; Fig. 4, 410, 420); and planarizing the deposited gate material proximate to the fin (page 7, paragraph 33; Fig. 4).

Claim 13 recites: The method of claim 11, further comprising: forming a dielectric layer over the top surface of the fin structure, the dielectric layer having a thickness ranging from about 150 Å to about 600 Å (page 5, paragraph 26; Fig. 2B, 140).

Claim 15 recites: The method of claim 11, further comprising: growing oxide layers on the first side surface and the second side surface of the fin structure, the oxide layers having a thickness ranging from about 10 Å to about 50 Å (page 6, paragraph 30, Fig. 3, 310).

Claim 21 recites: A method of manufacturing a semiconductor device, comprising: forming a fin on an insulating layer, the fin including side surfaces and a top surface and having a

height ranging from about 300 Å to about 1500 Å (page 5, paragraph 24; page 6, paragraph 27; Figs. 2A and 2B, 210); depositing a gate material over the fin, the gate material having a thickness ranging from about 300 Å to about 1500 Å (page 7, paragraph 31; Fig. 3, 320); etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin (page 7, paragraphs 32-34; Fig. 4, 410, 420); and removing the deposited gate material from over the top surface of the fin (page 7, paragraph 33; Fig. 4).

Claim 22 recites: The method of claim 21, further comprising: forming source and drain regions at ends of the fin; implanting impurities in the source and drain regions; and annealing the semiconductor device to activate the source and drain regions (page 6, paragraph 28; page 8, paragraph 36; Fig. 2A, 220, 230).

Claim 23 recites: The method of claim 21, further comprising: forming a dielectric cap on the top surface of the fin, the dielectric cap having a thickness ranging from about 150 Å to about 600 Å (page 5, paragraph 26; Fig. 2B, 140).

Claim 25 recites: The method of claim 21, further comprising: growing oxide layers on the opposite sides of the fin, the oxide layers having a thickness ranging from about 10 Å to about 50 Å (page 6, paragraph 30, Fig. 3, 310).

Claim 26 recites: A method of manufacturing a semiconductor device, comprising: forming

a fin having a height ranging from about 300 Å to about 1500 Å on an insulating layer (page 5, paragraph 24; page 6, paragraph 27; Figs. 2A and 2B, 210); forming gate dielectric layers having a thickness ranging from about 10 Å to about 50 Å on opposite sides of the fin (page 6, paragraph 30, Fig. 3, 310); depositing a gate material having a thickness ranging from about 300 Å to about 1500 Å over the fin and proximate the gate dielectric layers (page 7, paragraph 31; Fig. 3, 320); etching the gate material to form a first gate electrode and a second gate electrode on the opposite sides of the fin (page 7, paragraphs 32-34; Fig. 4, 410, 420); and removing a portion of the deposited gate material to electrically separate the first gate electrode from the second gate electrode (page 7, paragraph 33; Fig. 4).

Claim 27 recites: The method of claim 26, further comprising: forming source and drain regions at ends of the fin; implanting impurities in the source and drain regions; and annealing the semiconductor device to activate the source and drain regions (page 6, paragraph 28; page 8, paragraph 36; Fig. 2A, 220, 230).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 11-15 and 21-29 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Mathew et al. (U.S. Patent Publication No. 2003/0151077; hereinafter Mathew) in view of Gambino et al. (U.S. Patent No. 6,689,650; hereinafter Gambino).

VII. ARGUMENT

A. Rejection under 35 U.S.C. § 103 based on Mathew in view of Gambino

1. Claims 11, 12 and 14

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

With these principles in mind, claim 11 recites a method of manufacturing a semiconductor device that includes forming a fin structure on an insulating layer, the fin structure including a first side surface, a second side surface, and a top surface and having a thickness ranging from about 300 Å to about 1500 Å. The Final Office Action states that Mathew discloses forming a fin structure 24 on insulator 14 and points to Fig. 2 of Mathew for support (Final Office Action – page 3). Mathew, however, does not disclose that fin structure 24 has a thickness ranging from about 300 Å to about 1500 Å, as required by claim 11.

Claim 11 also recites depositing a gate material over the fin structure to a thickness ranging from about 300 Å to about 1500 Å, the gate material surrounding the top surface and the first and second side surfaces. The Final Office Action states that Mathew discloses depositing gate material 28 over fin structure 24 and points to Fig. 3 of Mathew for support (Final Office Action – page 3). Mathew, however, does not disclose or suggest that gate material 28 is deposited to a thickness ranging from about 300 Å to about 1500 Å, as required by claim 11.

Gambino has been used in the rejection of claim 11 to disclose annealing a semiconductor device to activate source and drain regions. Gambino, however, does not remedy the deficiencies in Mathew discussed above with respect to claim 11.

The Final Office Action admits that the combination of Mathew and Gambino does not disclose forming a fin structure having the claimed thickness or depositing a gate material to the claimed thickness (Final Office Action – page 4). The Final Office Action, however, states that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art and relies upon In re Aller, 105 USPQ 233 (CCPA 1995) for support (Final Office Action – pages 4-5). The Final Office Action further

alleges that the disclosed thicknesses of the fin structure and the gate material are not critical and that In re Aller supports the notion that the claimed ranges provide no support for patentability since Appellants have allegedly not disclosed anything that suggests the claimed ranges have any criticality associated with them (Final Office Action – page 5). Appellants respectfully disagree.

Initially, Appellants note that there is no requirement under 35 U.S.C. § 103 that a particular claim feature be "critical" in order for that claim to be patentable over the prior art. As discussed above, rejections based on 35 U.S.C. § 103 must rest on a factual basis. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 177-78 (CCPA 1967). In making such a rejection, the Examiner has the initial duty of supplying the requisite factual basis and may not, because of doubts that the invention is patentable, resort to speculation, unfounded assumptions, or hindsight reconstruction to supply deficiencies in the factual basis. Id.

In the present case, the Final Office Action has not advanced any factual basis as to why it would have been obvious to modify the combination of Mathew and Gambino to read on the features discussed above. Instead, the Examiner attempts to overcome the deficiencies in the combination of Mathew and Gambino by resorting to mechanical or per se rules of obviousness, such as that allegedly established by In re Aller. Such per se rules do not exist, however, and the reliance thereon by the Examiner to establish obviousness under 35 U.S.C. § 103 is improper. See In re Ochiai, 71 F.3d 1565, 1570, 37 USPQ2d 1127, 1132 (Fed. Cir. 1995); In re Wright, 343 F.2d 761, 769-70, 145 USPQ 182, 190 (CCPA 1965).

Mathew, as discussed above, is totally silent with regard to the thickness of fin structure 24 and the thickness of the deposited gate material 28. Claim 11, in contrast, recites specific ranges for the thickness of the fin structure and the gate material. Appellants assert that since

Mathew does not disclose any working ranges or values associated with the thickness of fin structure 24 or gate material 28, Mathew cannot be fairly construed to suggest forming a fin structure having the claimed thickness and depositing gate material having the claimed thickness absent impermissible hindsight.

Appellants also note that In re Aller involves determining whether making changes to a temperature range or changes to an acid concentration would be obvious. In re Aller at 235. Mathew, however, does not disclose any working range or value associated with the thickness of fin structure 24 or gate material 28. Therefore, Appellants assert that the determination in In re Aller regarding changes from one particular temperature and acid concentration to another temperature and acid concentration recited in a claim is not on point since Mathew does not disclose any values for either of the features discussed above. Therefore, Appellants assert that the allegation the claimed range would be obvious based on Mathew is based on impermissible hindsight due to, among other things, the lack of any ranges disclosed in Mathew.

Appellants further assert that the claimed ranges enable the method recited in claim 11 to achieve particular advantages with respect to manufacturing a semiconductor device having the desired properties, such as advantages associated with good short channel behavior of the semiconductor device (See Appellants' specification at paragraph 40 on page 9). In response to a similar argument made in the Request for Reconsideration filed March 12, 2005, the Advisory Action states that the portions of the specification pointed to above do not provide "a reason to have the specific ranges claimed" (Advisory Action – Continuation sheet).

Appellants maintain that the claimed features, including the claimed thickness of the fin structure and the gate material, enable the claimed invention to achieve particular advantages (as

pointed out at paragraph 40 on page 9 of Appellants' specification). Although Appellants did not specifically state, for example, that the claimed thicknesses allow the invention to achieve particular benefits/results, it should be understood that the claimed invention, including the claimed features with respect to the thickness of the fin structure and gate material, allow the invention to achieve the particular results.

Therefore, Appellants assert that the allegations with respect to the claimed thicknesses of the fin structure and gate material as being obvious based on Mathew and Gambino is mere speculation. Further, in the absence of any working range provided by Mathew, Appellants maintain that the use of In re Aller to somehow render the specifically recited ranges as obvious in view of Mathew and Gambino is inappropriate and does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, the combination of Mathew and Gambino does not disclose or suggest each of the features of claim 11.

In addition, even if, for the sake or argument, the combination of Mathew and Gambino could be fairly construed to disclose or suggest each of the features of claim 11, Appellants submit that the motivation relied upon for combining these references does not satisfy the requirements of 35 U.S.C. § 103.

For example, the Final Office Action states that it would have been obvious to combine Gambino with Mathew because the annealing activates the source/drain regions of the device (Final Office Action – page 4). This alleged motivation is merely a conclusory statement providing an alleged benefit of combining a feature of Gambino with Mathew. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, Appellants respectfully submit that the imposed rejection of claim 11 under 35 U.S.C. § 103 based on Mathew and Fried is improper. Accordingly, reversal of the rejection of claims 11, 12 and 14 is respectfully requested.

2. Claim 13

Claim 13 recites forming a dielectric layer over the top surface of the fin structure, the dielectric layer having a thickness ranging from about 150 Å to about 600 Å. Mathew discloses forming pad oxide layer 20 and/or nitride layer 22 over silicon structure 18 (Mathew – paragraph 17, lines 6-12). Mathew, however, does not disclose that the thickness of either of layers 20 and 22 ranges from about 150 Å to about 600 Å, as required by claim 13.

The Final Office Action admits that the combination of Mathew and Gambino does not disclose this feature, but relies upon In re Aller as providing support for the notion that the claimed range would be obvious. Appellants note that Mathew is totally silent with respect to the thickness of either of layers 20 and 22. Similar to the discussion above with respect to claim 11, Appellants assert that reliance on In re Aller to somehow render the specifically recited feature of claim13 as being obvious does not satisfy the requirements of 35 U.S.C. § 103.

Therefore, Appellants respectfully submit that the rejection of claim 13 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claim 13 is respectfully requested.

3. Claim 15

Claim 15 recites growing oxide layers on the first side surface and the second side surface of the fin structure, the oxide layers having a thickness ranging from about 10 Å to about 50 Å.

Mathew discloses forming gate dielectric 26 on opposite sides of silicon structure 18 (Mathew – paragraph 18, lines 2-5 and Fig. 3). Mathew, however, does not disclose or suggest that gate dielectric 26 has a thickness ranging from about 10 Å to about 50 Å, as required by claim 15.

The Final Office Action admits that the combination of Mathew and Gambino does not disclose this feature, but once again relies upon In re Aller as providing support for the notion that the claimed range would be obvious. Appellants note that Mathew is totally silent with respect to the thickness of gate dielectric 26. Similar to the discussion above with respect to claim 11, Appellants assert that reliance on In re Aller to somehow render the specifically recited feature of claim 15 as being obvious does not satisfy the requirements of 35 U.S.C. § 103.

Therefore, Appellants respectfully submit that the rejection of claim 15 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claim 15 is respectfully requested.

4. Claim 21

Claim 21 recites a method of manufacturing a semiconductor device that includes forming a fin on an insulating layer, the fin including side surfaces and a top surface and having a height ranging from about 300 Å to about 1500 Å. Claim 21 also recites depositing a gate material over the fin, the gate material having a thickness ranging from about 300 Å to about 1500 Å.

For reasons similar to those discussed above with respect to claim 11, the combination of Mathew and Gambino does not disclose or suggest these features of claim 21. Therefore, Appellants respectfully submit that the rejection of claim 21 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claim 21 is respectfully requested.

5. Claim 22

Claim 22 recites forming source and drain regions at ends of the fin; implanting impurities in the source and drain regions; and annealing the semiconductor device to activate the source and drain regions. The Final Office Action relies upon Gambino as disclosing annealing a semiconductor device to activate source and drain regions. The Final Office Action also states that it would have been obvious to combine Gambino with Mathew since the annealing activates the source/drain regions of the device (Final Office Action – page 4). Appellants respectfully disagree.

Similar to the discussion above with respect to claim 11, Appellants maintain that the alleged motivation for combining Gambino with Mathew is merely a conclusory statement providing an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, Appellants respectfully submit that the imposed rejection of claim 22 under 35 U.S.C. § 103 based on Mathew and Gambino is improper. Accordingly, reversal of the rejection of claim 22 is respectfully requested.

6. Claims 23 and 24

Claim 23 recites forming a dielectric cap on the top surface of the fin, the dielectric cap having a thickness ranging from about 150 Å to about 600 Å. For reasons similar to those discussed above with respect to claim 13, the combination of Mathew and Gambino does not disclose or suggest this feature.

For at least these reasons, Appellants respectfully submit that the imposed rejection of

claim 23 under 35 U.S.C. § 103 based on Mathew and Gambino is improper. Accordingly, reversal of the rejection of claims 23 and 24 is respectfully requested.

7. Claim 25

Claim 25 recites growing oxide layers on the opposite sides of the fin, the oxide layers having a thickness ranging from about 10 Å to about 50 Å. For reasons similar to those discussed above with respect to claim 15, the combination of Mathew and Gambino does not disclose or suggest this feature.

For at least these reasons, Appellants respectfully submit that the imposed rejection of claim 25 under 35 U.S.C. § 103 based on Mathew and Gambino is improper. Accordingly, reversal of the rejection of claim 25 is respectfully requested.

8. Claims 26, 28 and 29

Claim 26 recites a method of manufacturing a semiconductor device that includes forming a fin having a height ranging from about 300 Å to about 1500 Å on an insulating layer; forming gate dielectric layers having a thickness ranging from about 10 Å to about 50 Å on opposite sides of the fin; and depositing a gate material having a thickness ranging from about 300 Å to about 1500 Å over the fin and proximate the gate dielectric layers. These features are similar to features recited in claims 11 and 15.

As discussed above with respect to claims 11 and 15, the combination of Mathew and Gambino does not disclose or suggest these features. In contrast, Mathew is totally silent with respect to the height of fin structure 24, the thickness of gate material 28 and the thickness of

dielectric layer 26. The Final Office Action admits that the combination of Mathew and Gambino does not disclose these features, but once again relies upon In re Aller as providing support for the notion that the claimed ranges would be obvious. Similar to the discussion above with respect to claims 11 and 15, Appellants assert that reliance on In re Aller to somehow render the specifically recited features of claim 26 as being obvious does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, Appellants respectfully submit that the imposed rejection of claim 26 under 35 U.S.C. § 103 based on Mathew and Gambino is improper. Accordingly, reversal of the rejection of claims 26, 28 and 29 is respectfully requested.

9. Claim 27

Claim 27 recites a feature similar to claim 22. For reasons similar to those discussed above with respect to claim 22, Appellants respectfully submit that the imposed rejection of claim 27 under 35 U.S.C. § 103 is improper. Accordingly, reversal of the rejection of claim 27 is respectfully requested.

VIII. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 11-15 and 21-29.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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IX. APPENDIX

11. A method of manufacturing a semiconductor device, comprising:

forming a fin structure on an insulating layer, the fin structure including a first side surface, a second side surface, and a top surface and having a thickness ranging from about 300 Å to about 1500 Å;

forming source and drain regions at ends of the fin structure;

depositing a gate material over the fin structure to a thickness ranging from about 300 Å to about 1500 Å, the gate material surrounding the top surface and the first and second side surfaces;

etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin; and

planarizing the deposited gate material proximate to the fin.

12. The method of claim 11, wherein the forming source and drain regions comprises:

depositing a layer of silicon, germanium, or combination of silicon and germanium, and

patterning and etching the deposited layer to form the source and drain regions, the method further comprising:

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

13. The method of claim 11, further comprising:

forming a dielectric layer over the top surface of the fin structure, the dielectric layer having a thickness ranging from about 150 Å to about 600 Å.

14. The method of claim 13, wherein the planarizing includes:

polishing the gate material so that no gate material remains above the dielectric layer.

15. The method of claim 11, further comprising:

growing oxide layers on the first side surface and the second side surface of the fin structure, the oxide layers having a thickness ranging from about 10 Å to about 50 Å.

21. A method of manufacturing a semiconductor device, comprising:

forming a fin on an insulating layer, the fin including side surfaces and a top surface and having a height ranging from about 300 Å to about 1500 Å;

depositing a gate material over the fin, the gate material having a thickness ranging from about 300 Å to about 1500 Å;

etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin; and

removing the deposited gate material from over the top surface of the fin.

22. The method of claim 21, further comprising:

forming source and drain regions at ends of the fin;

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

23. The method of claim 21, further comprising:

forming a dielectric cap on the top surface of the fin, the dielectric cap having a thickness ranging from about 150 Å to about 600 Å.

24. The method of claim 23, wherein the removing includes:

polishing the gate material down to the dielectric cap.

25. The method of claim 21, further comprising:

growing oxide layers on the opposite sides of the fin, the oxide layers having a thickness ranging from about 10 Å to about 50 Å.

26. A method of manufacturing a semiconductor device, comprising:

forming a fin having a height ranging from about 300 Å to about 1500 Å on an insulating layer;

forming gate dielectric layers having a thickness ranging from about 10 Å to about 50 Å on opposite sides of the fin;

depositing a gate material having a thickness ranging from about 300 Å to about 1500 Å over the fin and proximate the gate dielectric layers;

etching the gate material to form a first gate electrode and a second gate electrode on the opposite sides of the fin; and

removing a portion of the deposited gate material to electrically separate the first gate electrode from the second gate electrode.

27. The method of claim 26, further comprising:

forming source and drain regions at ends of the fin;

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

28. The method of claim 26, further comprising:

forming a dielectric cap on a top surface of the fin.

29. The method of claim 28, wherein the removing includes:

polishing the gate material down to the dielectric cap.